

**IN THE CLAIMS:**

The following listing of claims will replace all prior versions, and listings, of claims in the application.

1-15. (Cancelled)

16. (Currently Amended) A method comprising:  
generating a constant reference voltage;  
generating a threshold voltage component, wherein the threshold voltage component approximates a threshold voltage of an NMOS process over variations in operating temperature and/or variations in transistor fabrication parameters;  
generating a composite voltage that is a sum of the constant reference voltage and the threshold voltage component; and  
applying the composite voltage to a gate of a tail current transistor of a ~~voltage level detector~~ differential input stage, thereby producing a trip point ~~an offset voltage of the voltage level detector~~ differential input stage that is substantially independent of ~~the~~ operating temperature and/or ~~the~~ variations in transistor fabrication parameters, ~~the trip point thereby remaining substantially constant;~~  
~~wherein the offset voltage of the differential input stage is proportional to the constant reference voltage.~~

17. (Cancelled)

18. (Currently Amended) The method of claim 16, wherein the threshold voltage component of the composite voltage turns on the tail current transistor despite ~~the~~ variations in operating temperature and/or ~~the~~ variations in transistor fabrication parameters.

19. (Previously Presented) The method of claim 18, wherein the constant reference voltage component of the composite voltage produces a tail current for the voltage level detector that is proportional to a beta for the NMOS process.

20-24. (Cancelled)

25. (Currently Amended) The method of claim 16, wherein ~~the voltage level detector is~~ differential input stage is comprised in one of:

- a differential amplifier; and
- a voltage level detector.

26. (Currently Amended) The method of claim ~~25~~ 16, wherein ~~an~~ the offset voltage of the ~~differential amplifier~~ remains substantially constant despite the variations in operating temperature and/or the variations in transistor fabrication parameters.

27. (New) A device comprising:

a voltage level detector comprising an NMOS tail current transistor;  
a voltage generator configured to deliver a voltage to a gate of the tail current transistor; and  
a differential pair of NMOS transistors whose sources are configured to couple to a drain of the tail current transistor, wherein a channel-width-to-length ratio of a first one of the differential pair of NMOS transistors differs from a channel-width-to-length ratio of the second one of the differential pair of NMOS transistors;

wherein a first component of the voltage is approximately equal to a threshold voltage (V<sub>t</sub>) of NMOS transistors comprised in the device; and

wherein a second component of the voltage is approximately constant with respect to variations in operating temperature and/or variations in transistor fabrication parameters.

28. (New) The device of claim 27, wherein the voltage generator comprises a diode-connected transistor and a constant current sink configured to produce the first component of the voltage;

wherein a source of the diode-connected transistor is configured to couple to an input of the constant current sink;

wherein an output of the constant current sink is configured to couple to a negative supply;

wherein a configuration of channel-width-to-length ratio (W/L) of the diode-connected transistor, in conjunction with a current (I) drawn by the constant current sink, satisfies  $(I/\beta)^2 \ll V_t$ ; and

wherein the first component of the voltage is produced as a gate-source voltage of the diode-connected transistor.

29. (New) The device of claim 28, wherein the voltage generator further comprises a bandgap voltage reference having an output configured as the second component of the voltage.

30. (New) The device of claim 29, wherein the voltage generator further comprises an amplifier and a PMOS transistor configured to produce a sum of the first and second components of the voltage at a gate of the diode-connected transistor;

wherein an output of the bandgap voltage reference is configured to couple to an inverting (negative) input of the amplifier;

wherein the source of the diode-connected transistor is configured to couple to the non-inverting (positive) input of the amplifier;

wherein an output of the amplifier is configured to couple to a gate of the PMOS transistor;

wherein a drain of the PMOS transistor is configured to couple to the gate and drain of the diode-connected transistor; and

wherein a source of the PMOS transistor is configured to couple to a positive supply.

31. (New) The device of claim 27, wherein the first component of the voltage provides a minimum voltage required to turn on the tail current transistor, substantially unaffected by variations in operating temperature and/or variations in transistor fabrication parameters.

32. (New) The device of claim 27, wherein the second component of the voltage provides a constant effective voltage ( $V_{eff}$ ) for the tail current transistor, the tail current transistor thereby producing the tail current ( $I_t$ ) proportional to an NMOS process beta parameter according to:  $I_t = (\beta/2)*(V_{eff})^2$ .

33. (New) The device of claim 27, wherein a trip point of the voltage level detector is substantially constant despite variations in operating temperature as well as variations in transistor fabrication parameters.

34. (New) A device comprising:  
a differential amplifier comprising an NMOS tail current transistor; and  
a voltage generator configured to deliver a voltage to a gate of the tail current transistor, the voltage generator comprising:  
a constant current sink having an output configured to couple to a negative supply; and  
a diode-connected transistor having a source configured to couple to an input of the constant current sink;  
wherein the constant current sink and the diode-connected transistor are configured to produce a first component of the voltage as a gate-source voltage of the diode-connected transistor;  
wherein a configuration of channel-width-to-length ratio (W/L) of the diode-connected transistor, in conjunction with a current (I) drawn by the constant current sink, satisfies  $(I/\beta)^2 \ll V_t$ ;  
wherein the first component of the voltage is approximately equal to a threshold voltage ( $V_t$ ) of NMOS transistors comprised in the device over variations

in operating temperature as well as variations in transistor fabrication parameters; and

wherein a second component of the voltage is approximately constant with respect to the variations in operating temperature and/or the variations in transistor fabrication parameters.

35. (New) The device of claim 34, wherein the voltage generator further comprises a bandgap voltage reference configured to produce the second component of the voltage as its output.

36. (New) The device of claim 35, wherein the voltage generator further comprises an amplifier and a PMOS transistor configured to produce a sum of the first and second components of the voltage at a gate of the diode-connected transistor;

wherein an output of the bandgap voltage reference is configured to couple to a negative (inverting) input of the amplifier;

wherein the source of the diode-connected transistor is configured to couple to the positive (non-inverting) input of the amplifier;

wherein an output of the amplifier is configured to couple to a gate of the PMOS transistor;

wherein a drain of the PMOS transistor is configured to couple to the gate and drain of the diode-connected transistor; and

wherein a source of the PMOS transistor is configured to couple to a positive supply.

37. (New) The device of claim 34, wherein the first component of the voltage provides a minimum voltage required to turn on the tail current transistor, substantially unaffected by the variations in operating temperature and/or the variations in transistor fabrication parameters.

38. (New) The device of claim 34, wherein the second component of the voltage provides a constant effective voltage ( $V_{eff}$ ), for the tail current transistor, the tail current

transistor thereby producing the tail current ( $I_t$ ), proportional to an NMOS process beta parameter according to:  $I_t = (\beta/2) * (V_{eff})^2$ .

39. (New) The device of claim 34, wherein an offset voltage of the differential amplifier is substantially unaffected by the variations in operating temperature and/or the variations in transistor fabrication parameters, thereby remaining substantially constant.

40. (New) A device comprising:

a voltage level detector comprising an NMOS tail current transistor; and

a voltage generator configured to deliver a voltage to a gate of the tail current transistor, the voltage generator comprising:

a constant current sink having an output configured to couple to a negative supply; and

a diode-connected transistor having a source configured to couple to an input of the constant current sink;

wherein the constant current sink and the diode-connected transistor are configured to produce a first component of the voltage as a gate-source voltage of the diode-connected transistor;

wherein a configuration of channel-width-to-length ratio (W/L) of the diode-connected transistor, in conjunction with a current ( $I$ ) drawn by the constant current sink, satisfies  $(I/\beta)^2 \ll V_t$ ; and

wherein the first component of the voltage is approximately equal to a threshold voltage ( $V_t$ ) of NMOS transistors comprised in the device; and

wherein a second component of the voltage is approximately constant with respect to variations in operating temperature and/or variations in transistor fabrication parameters.

41. (New) The device of claim 40, wherein the voltage generator further comprises a bandgap voltage reference configured to produce the second component of the voltage as its output.

42. (New) The device of claim 41, wherein the voltage generator further comprises an amplifier and a PMOS transistor configured to produce a sum of the first and second components of the voltage at a gate of the diode-connected transistor; wherein an output of the bandgap voltage reference is configured to couple to an inverting (negative) input of the amplifier; wherein the source of the diode-connected transistor is configured to couple to the non-inverting (positive) input of the amplifier; wherein an output of the amplifier is configured to couple to a gate of the PMOS transistor; wherein a drain of the PMOS transistor is configured to couple to the gate and drain of the diode-connected transistor; and wherein a source of the PMOS transistor is configured to couple to a positive supply.

43. (New) The device of claim 40, wherein the first component of the voltage provides a minimum voltage required to turn on the tail current transistor, substantially unaffected by the variations in operating temperature and/or the variations in transistor fabrication parameters.

44. (New) The device of claim 40, wherein the second component of the voltage provides a constant effective voltage ( $V_{eff}$ ) for the tail current transistor, the tail current transistor thereby producing the tail current ( $I_t$ ) proportional to an NMOS process beta parameter according to:  $I_t = (\beta/2) * (V_{eff})^2$ .

45. (New) The device of claim 40, further comprising a differential pair of NMOS transistors whose sources are coupled to a drain of the tail current transistor, wherein a channel-width-to-length ratio of a first one of the differential pair of NMOS transistors differs from a channel-width-to-length ratio of the second one of the differential pair of NMOS transistors.

46. (New) The device of claim 40, wherein a trip point of the voltage level detector is substantially constant despite the variations in operating temperature and/or the variations in transistor fabrication parameters.

47. (New) A device comprising:

a voltage level detector comprising an NMOS tail current transistor; and

a voltage generator configured to deliver a voltage to a gate of the tail current transistor;

wherein a first component of the voltage is approximately equal to a threshold voltage ( $V_t$ ) of NMOS transistors comprised in the device; and

wherein a second component of the voltage is approximately constant with respect to variations in operating temperature and/or variations in transistor fabrication parameters; and

wherein the second component of the voltage provides a constant effective voltage ( $V_{eff}$ ) for the tail current transistor, the tail current transistor thereby producing a tail current ( $I_t$ ) proportional to an NMOS process beta parameter according to:  $I_t = (\beta/2) * (V_{eff})^2$ .

48. (New) The device of claim 47, wherein a trip point of the voltage level detector is substantially constant despite variations in the operating temperature and/or the variations in transistor fabrication parameters.

49. (New) The device of claim 47, wherein the first component of the voltage provides a minimum voltage required to turn on the tail current transistor, substantially unaffected by the variations in operating temperature and/or the variations in transistor fabrication parameters.

50. (New) A device comprising:

a differential amplifier comprising an NMOS tail current transistor; and

a voltage generator coupled to a gate of the tail current transistor;

wherein the voltage generator is configured to deliver a voltage to the gate of the tail current transistor;

wherein a first component of the voltage is approximately equal to a threshold voltage ( $V_t$ ) of NMOS transistors comprised in the device over variations in operating temperature as well as variations in transistor fabrication parameters;

wherein a second component of the voltage is approximately constant with respect to variations in operating temperature and/or variations in transistor fabrication parameters; and

wherein the second component of the voltage provides a constant effective voltage ( $V_{eff}$ ), for the tail current transistor, the tail current transistor thereby producing the tail current ( $I_t$ ), proportional to an NMOS process beta parameter according to:  $I_t = (\beta/2) * (V_{eff})^2$ .

51. (New) The device of claim 50, wherein the first component of the voltage provides a minimum voltage required to turn on the tail current transistor, substantially unaffected by the variations in operating temperature and/or the variations in transistor fabrication parameters.

52. (New) The device of claim 50, wherein an offset voltage of the differential amplifier is substantially unaffected by the variations in operating temperature and/or the variations in transistor fabrication parameters, thereby remaining substantially constant.

53. (New) The device of claim 50, wherein the voltage generator comprises:  
a constant current sink having an output configured to couple to a negative supply;  
a diode-connected NMOS transistor having a source configured to couple to an input of the constant current sink; and  
a bandgap voltage reference configured to produce the second component of the voltage as its output;

wherein the constant current sink and the diode-connected NMOS transistor are configured to produce the first component of the voltage as gate-source voltage of the diode-connected transistor; and

wherein a configuration of channel-width-to-length ratio (W/L) of the diode-connected transistor, in conjunction with a current (I) drawn by the constant current sink, satisfies  $(I/\beta)^2 \ll V_t$ .

54. (New) The device of claim 53, wherein the voltage generator further comprises an amplifier and a PMOS transistor configured to produce a sum of the first and second components of the voltage at a gate of the diode-connected transistor;

wherein an output of the bandgap voltage reference is configured to couple to a negative (inverting) input of the amplifier;

wherein the source of the diode-connected transistor is configured to couple to the positive (non-inverting) input of the amplifier;

wherein an output of the amplifier is configured to couple to a gate of the PMOS transistor;

wherein a drain of the PMOS transistor is configured to couple to the gate and drain of the diode-connected transistor; and

wherein a source of the PMOS transistor is configured to couple to a positive supply.